CLAIMS

What is claimed is:

1. A method comprising:

initializing a serial point to point link that communicatively couples an integrated circuit (IC) device to another IC device, by transferring a training sequence of symbols over the link;

programming a plurality of registers of the IC device to i) set a test symbol data pattern and ii) configure a lane transmitter for the link;

programming a start bit in a register of the IC device, to request that the link be placed in a measurement mode; and

the IC device, in said measurement mode, instructs said another IC device to enter a loopback mode for the link in which symbols received over the link are looped back, transmits a sequence of test symbols over the link and evaluates a looped back version of the sequence for errors, wherein the sequence of test symbols have a data pattern, and are transmitted, as configured in the plurality of registers.

2. The method of claim 1 wherein the initializing further comprises determining how many lanes are available for operation in said link.

3. The method of claim 2 wherein the IC device indicates that the link is ready for normal operation with a determined number of lanes, and wherein the programming of the start bit is performed by a host while the link is ready for normal operation.

4. The method of claim 1 wherein the IC device, prior to entering the measurement mode for the link, makes the following PCI Express state transitions: L0 to Recovery to L0 to Polling Compliance.

5. The method of claim 1 wherein the IC device, upon exiting the measurement mode for the link, makes the following PCI Express state transitions: Polling Compliance to Loopback Exit to Detect Quiet.

6. The method of claim 1 further comprising:

programming by a host a stop bit in a register of the IC device, to request that the link exits the measurement mode.

7. The method of claim 6 wherein the programming of the start and stop bits include invoking PCI Express configuration write commands.

8. The method of claim 1 wherein the IC device, in the measurement mode, instructs said another IC device to enter the loopback mode by transmitting a PCI Express TS1/TS2 Ordered Set over the link.

9. An integrated circuit (IC) device, comprising:

an analog front end (AFE) transmit block to convert input symbols into a stream of information to be transmitted over a serial point to point link;

an AFE receive block to receive a stream of information over the serial point to point link; and

measurement mode circuitry (MMC) to provide the AFE transmit block a sequence of test symbols to be transmitted over the link while the link is operating in a measurement mode, the MMC to evaluate a sequence of test symbols, received by the AFE receive block over said link, for errors,

wherein the link is to enter the measurement mode from a normal mode in response to a predefined bit of a register of the IC device being programmed, the IC device having one or more programmable registers whose bits instruct the MMC to change a data pattern in the sequence of test symbols and one of a) an autoinvert setting, b) a default setting for an inverted lane of the link, c) an inversion setting, and d) initial disparity, for the link.

10. The IC device of claim 9 wherein the MMC is to log an error in the received sequence of test symbols in a software-accessible register of the IC device.

11. The IC device of claim 9 wherein upon entering the measurement mode, the MMC is to instruct another IC device at another end of the link to loop the transmitted sequence of test symbols back over the same lane of the link.

12. The IC device of claim 11 wherein the MMC is to provide a training sequence of symbols that is to be transmitted by the AFE transmit block upon

the link entering the measurement mode and that is recognizable by said another IC device as including a request to place said another end of the link in a loopback mode.

13. The IC device of claim 11 wherein the MMC is to provide a PCI Express TS1/TS2 Ordered Set that is to be transmitted by the AFE transmit block upon the link entering the measurement mode and that includes a loopback bit being set.

14. The IC device of claim 9 wherein the sequence of test symbols includes a PCI Express SKP Ordered Set followed by a compliance pattern.

15. The IC device of claim 9 wherein the link is to remain in the measurement mode and is not to exit the measurement mode until a predefined bit of a register of the IC device has been programmed.

16. The IC device of claim 9 wherein the bit of the register is software-accessible during the normal mode via a configuration write command.

17. A system comprising:

a processor;

a main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having link interface circuitry that supports a serial point to point link, the circuitry includes

an analog front end (AFE) transmit block to convert input symbols into a stream of information to be transmitted over the link;

an AFE receive block to receive a stream of information over the link; and

measurement mode circuitry (MMC) to provide the AFE transmit block a sequence of test symbols to be transmitted over the link while the link is operating in a measurement mode, the MMC to evaluate a sequence of test symbols, received by the AFE receive block over said link, for errors,

wherein the link is to enter the measurement mode from a normal mode in response to a predefined bit of a register of the IC device being programmed, the IC device having one or more programmable registers whose bits instruct the MMC to change a data pattern in the sequence of test symbols and one of a) an autoinvert setting, b) a default setting for an inverted lane of the link, c) an inversion setting, and d) initial disparity, for the link.

18. The system of claim 17 wherein upon entering the measurement mode, the MMC is to instruct another IC device at another end of the link to loop the transmitted sequence of test symbols back over the same lane of the link.

19. The system of claim 18 wherein the MMC is to provide a training sequence of symbols that is to be transmitted by the AFE transmit block upon the link entering the measurement mode and that is recognizable by said another IC device as including a request to place said another end of the link in a loopback mode.

20. The system of claim 17 wherein the link is to remain in the measurement mode and is not to exit the measurement mode until a predefined bit of a register of the IC device has been programmed.

21. The system of claim 17 wherein the bit of the register is software-accessible during the normal mode via a processor-initiated configuration write command.

22. The system of claim 18 wherein the IC device is a memory controller hub.

23. The system of claim 19 wherein the IC device is an I/O controller hub that communicatively couples the processor to peripheral devices.